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THE DESIGN OF A SOLID-STATE REPLACEMENT FOR CHASSIS 5 OF THE AI--ETC(U)
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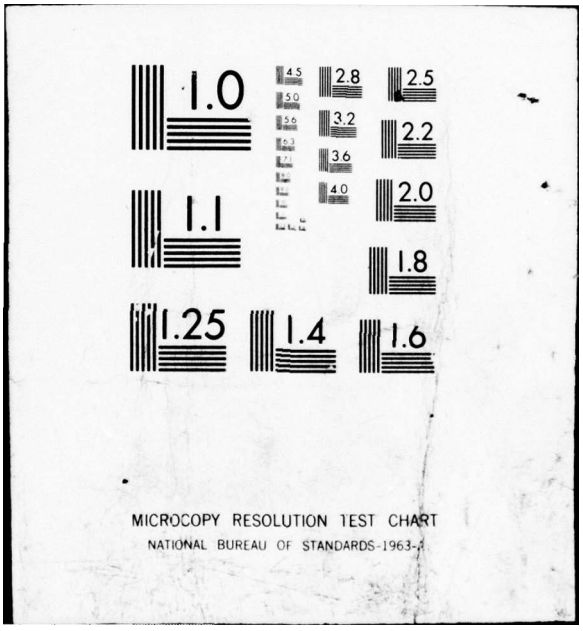
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FINAL REPORT

THE DESIGN OF A SOLID-STATE REPLACEMENT FOR CHASSIS 5 OF THE AIM-4A GUIDANCE UNIT

August 1972

Prepared for
WARNER ROBINS AIR MATERIEL AREA
ROBINS AIR FORCE BASE, GEORGIA
under Contract F09603-71-A-3749-0004

ARINC RESEARCH CORPORATION

(9) FINAL REPORT

(6) THE DESIGN OF A SOLID-STATE REPLACEMENT FOR CHASSIS 5 OF THE AIM-4A GUIDANCE UNIT

(11) August 1972

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Prepared for
Warner Robins Air Materiel Area
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ABSTRACT

Under Contract F09603-71-A-3749-0004, ARINC Research Corporation has designed and tested a replacement module for Chassis 5 in the AIM-4A guidance unit. The replacement incorporates both integrated circuits and transistors, and was designed to be directly interchangeable with the vacuum tube chassis without the necessity of other system modifications.

Two prototype models of the redesigned chassis were fabricated. Testing included functional and environmental tests. Captive flight tests of the prototype are planned for a later time. The functional and environmental tests have indicated that the solid-state module is a direct replacement for the vacuum-tube model.

CONTENTS

CHAPTER ONE

INTRODUCTION

The AIM-4A is a radar-guided air-to-air missile in the Falcon series; in addition, a motorless version of the missile is used as an unlaunched "Weapon System Evaluator Missile" (WSEM) for the F-102 aircraft.

Chassis 5 of the AIM-4A guidance system has exhibited a high failure rate. With the primary purpose of improving the reliability of Chassis 5, Warner Robins Air Materiel Area (WRAMA) authorized ARINC Research Corporation, by Contract F09603-71-3749-0004, to redesign the chassis, replacing the vacuum tubes with solid-state devices as the active elements in the circuits.

The design goal was a module that is directly interchangeable with the vacuum tube chassis. This objective required the conversion of presently available, tube-oriented, power-supply levels within the chassis to voltage levels suitable for powering semiconductor circuits.

CHAPTER TWO

TECHNICAL APPROACH

2.1 DELIVERABLE PRODUCTS

The deliverable products required under the contract for this design effort are (1) prototype hardware suitable for environmental and flight testing and (2) a documentation package suitable for the competitive procurement of production hardware. Section 2.2 discusses the several tasks involved in the design and preparation of these items.

2.2 CONTRACTUAL TASKS AND APPROACH TO TASK PERFORMANCE

The tasks enumerated in the contract document and the approach employed by ARINC Research for performance of the work are summarized below.

Task A: "Study the AIM-4A system interface requirements"

A description of the operation of Chassis 5 was obtained from the following sources: (1) applicable Technical Orders, (2) the Chassis 5 specification, (3) measurements and oscilloscope photographs taken from the console-operated missile in the field, and (4) bench tests of a present version of Chassis 5.

Task B: "Design a preliminary electrical and mechanical solid-state replacement for the existing vacuum tube circuits in Chassis 5 including DC-DC converters as required to provide power to the solid-state circuits".

The first step in the preliminary design of Chassis 5 circuitry was the selection of solid-state devices based on performance, reliability, cost, size, and power-consumption tradeoffs. Upon completion of the device-selection process, a theoretical design of the system, including power supply converters, was accomplished.

Task C: "Construct and test breadboards to prove the ability of the preliminary design to provide the desired function."

Breadboard models were constructed to provide the initial tests of the circuit designs. They were so constructed as to perform the electrical functions of the design without necessarily conforming to the physical constraints of the missile; also, the construction techniques were of a nature facilitating the extensive modifications to be expected in an initial design. Tests were conducted with laboratory test equipment to simulate the interface with the missile.

Task D: "Construct two prototype units providing for mechanical and electrical interchangeability with the existing Chassis 5."

Prototypes of the finalized Chassis 5 circuits were constructed after tests and modifications of the breadboard models. The prototype units incorporate printed circuit boards and are capable of being physically plugged into the AIM-4A guidance unit for flight tests.

Task E: "Bench test the prototypes to prove functional capability".

Completed prototype units were bench-tested to verify satisfactory operation. Operation of the prototype provided some indication of the repeatability of the design, previously checked in breadboard form only.

Task F: "Environmental test one of the prototype units to demonstrate capability of the flight environment. Deliver the other prototype unit to WRAMA for flight test and provide engineering support for ten (10) working days of the flight tests."

Environmental tests of the prototype consisted of temperature and vibration tests at levels of stress indicated in the present module specification. The flight tests will provide assurance that the design will perform in the total flight environment.

Task G: "Refurbish the environmental prototype to make ready for additional flight tests."

Because of design problems in the time-discriminator and oscillator circuits, the environmental test prototype — the first built — was not suitable for operating in a missile. The unit was extensively modified to correct the deficiencies; however, the changes rendered the prototype much poorer in mechanical integrity than the second and final prototype, which employed a printed circuit board with the circuit modifications incorporated.

Task H: "Provide assurance that the new solid-state Chassis 5 is completely interchangeable with the old vacuum tube version without requiring any other changes in the weapon system whatever."

This item will be satisfied by the inherent design of the new module and the accumulation of test data indicating fulfillment of the requirement.

Task I: "Final Engineering Report containing all design information, block diagrams, schematics, bill of material, description of theory of operation, and test requirement document. There shall also be provided a data package suitable for competitive procurement of the solid-state Chassis 5. The data package shall include drawings and specifications."

The information and materials required by Task I are supplied in this final report and the data package which is submitted separately.

CHAPTER THREE

CIRCUIT DESCRIPTION

3.1 FUNCTIONS AND CHARACTERISTICS OF CHASSIS 5 CIRCUITRY

The functions of the circuitry in Chassis 5 are to synchronize the Missile Range Gate (MRG) pulse with the Radar Range Gate (RRG) pulse during captive flight and to provide an MRG which tracks the target video pulse during free flight. The Missile Range Gate permits the missile's radar receiver to function only during a small period representing the range to the target. Gating of the target pulse produces two advantages: (1) the signal-to-noise ratio of the system is improved, and (2) tendencies to track extraneous targets are reduced.

During captive flight, synchronization with the Radar Range Gate is achieved by a slewing* voltage developed in an aircraft-mounted assembly known as the 106 unit. Upon launch, the control system in Chassis 5 maintains the Missile Range Gate lock on the target pulse position. If the synchronization of target pulse and Missile Range Gate is lost for a period exceeding the memory capability of Chassis 5, reacquisition during missile flight is not possible. The memory feature causes the Missile Range Gate to maintain its position for some small time period during which no target video is received.

The desirable operating characteristics of the circuits in Chassis 5 can be summarized as follows:

- Fast lock-on when being slewed by an external voltage
- Ability to track an accelerating target
- A long memory capability

3.2 MAIN COMPONENTS

The block diagram for Chassis 5 is shown in Figure 1. A summary of internal test-point waveforms is provided in Appendix A, which is classified CONFIDENTIAL and transmitted separately as a supplement to this report. A list of interface characteristics is given in Appendix B. Descriptions of the main components of Chassis 5 are presented below.

(1) The Voltage-Controlled Oscillator is a square-wave generator with a crystal-stabilized frequency. The frequency is electrically adjustable by a control voltage which changes the capacity of a varactor diode in the crystal circuit.

*Slewing refers to the coarse correction signal applied to the Chassis 5 circuitry to achieve initial lock-on to the RRG. In the vacuum tube model, a -250 volt signal is received from the 106 box to indicate that the system is slewing. Upon the completion of external slewing, the -250 volt signal is removed and internal tracking is enabled. The solid-state module does not switch from one mode to another; rather, both external and internal error signals are simultaneously summed in the same amplifier.

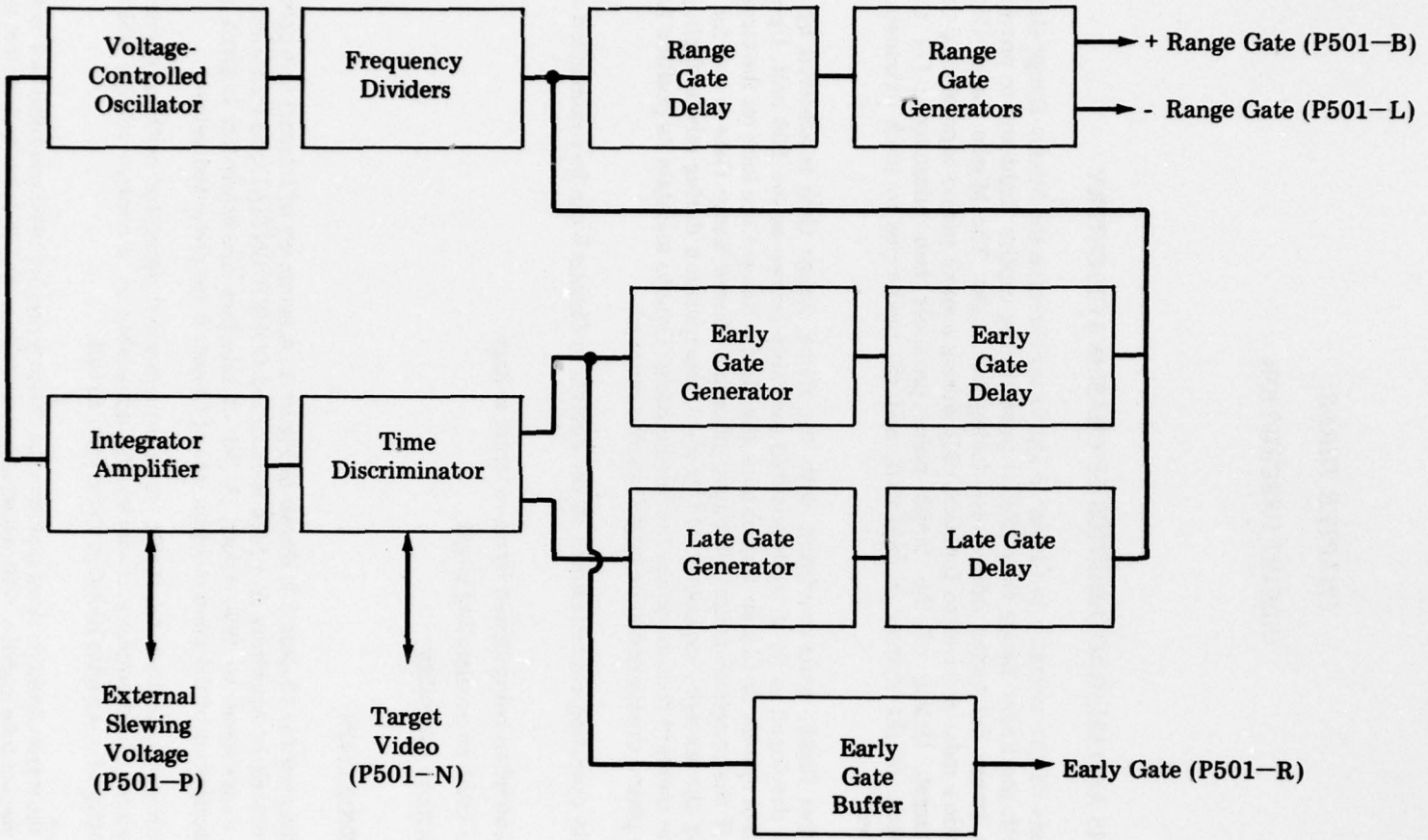


Figure 1. **BLOCK DIAGRAM OF CHASSIS 5**

(2) Frequency Dividers are used to divide the frequency of the Voltage-Controlled Oscillator down to the radar pulse repetition frequency (prf). The combination of a high-frequency oscillator and frequency dividers is used because crystal oscillator circuits are more practical at higher frequencies than at the radar prf.

(3) The Range Gate Delay, Early Gate Delay, and Late Gate Delay circuits are solid-state monostable multivibrators (one-shots) which position the Range Gates, Early Gate, and Late Gate, respectively. The Range Gate Delay is adjusted during acceptance testing to compensate for system delays.

(4) Each of the Range Gate Generators consists of a one-shot, which forms a pulse of the proper duration, and a pulse amplifier, which produces the required amplitude.

(5) The Early and Late Gate Generators are one-shots which are triggered by the Early and Late Gate Delay one-shots to produce pulses of the proper phase and duration for the operation of the Time Discriminator Circuit.

(6) The Time Discriminator Circuit produces an analog output that is related to the relative time position of the target video pulse and the early and late gates.

(7) The Integrator Amplifier filters the output of the Time Discriminator Circuit and contributes the proper amount of phase lag for optimum servo response. Presence of the integration function in the servo loop makes it possible to achieve the velocity memory function. The output of the Integrator Amplifier serves as the control voltage for the Voltage Controlled Oscillator, thus closing the control loop. The external slewing voltage is connected to the noninverting input of the Integrator Amplifier.

(8) The Early Gate Buffer is a transistor switch which generates a positive 5-volt pulse used as the Missile Range Gate (MRG) pulse in the 106 box.

3.3 THEORY OF OPERATION

The 106 unit generates a missile lock-on voltage by synchronizing a square wave to the Radar Range Gate and developing an error voltage based on the phase difference between the Missile Range Gate and the square wave. This feature is illustrated in Figure 2. When the Missile Range Gate occurs in the 180-degree interval after the Radar Range Gate, a positive lock-on voltage is developed which decreases the Chassis 5 clock frequency until lock-on is achieved. When the Missile Range Gate occurs in the 180-degree interval before the Radar Range Gate — and, thus, before the leading edge of the square wave — the result is a negative lock-on voltage which increases the clock frequency of Chassis 5 until lock-on is achieved. When lock-on is reached — i.e., when the Missile Range Gate is synchronized with the Radar Range Gate — the lock-on voltage reduces to close to zero. A level-sensing circuit in the 106 unit senses the nulled lock-on voltage and energizes a lock-on relay which lights the lock-on indicator light and switches off the -250-volt lock-on voltage fed to Chassis 5.

The target-tracking signal is developed in Chassis 5 in a manner similar to that used in the 106 unit, as seen in Figure 3. The Missile Range Gate, having been positioned over the target video pulse by being synchronized to the Radar Range Gate, must track the target video position by nulling out errors produced by target acceleration or drifts in missile circuit parameters. The main difference between the Chassis 5 and 106 unit circuits is in the early and late gate pulses used to produce frequency control signals of the proper polarity. In Chassis 5, narrower pulses are employed because the Missile Range Gate is initially positioned by the 106 unit and need only track the comparatively slow relative movements of the target video pulse caused by acceleration and drift. A square-wave system such as that used in the 106 unit might seem desirable for the missile because of the potential for

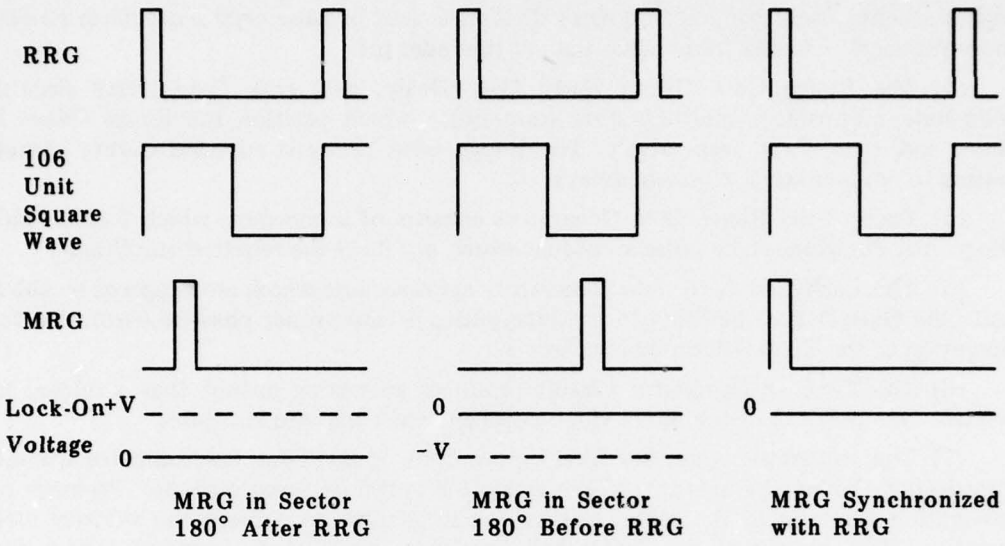


Figure 2. **EXTERNAL SLEWING VOLTAGE CONDITIONS**

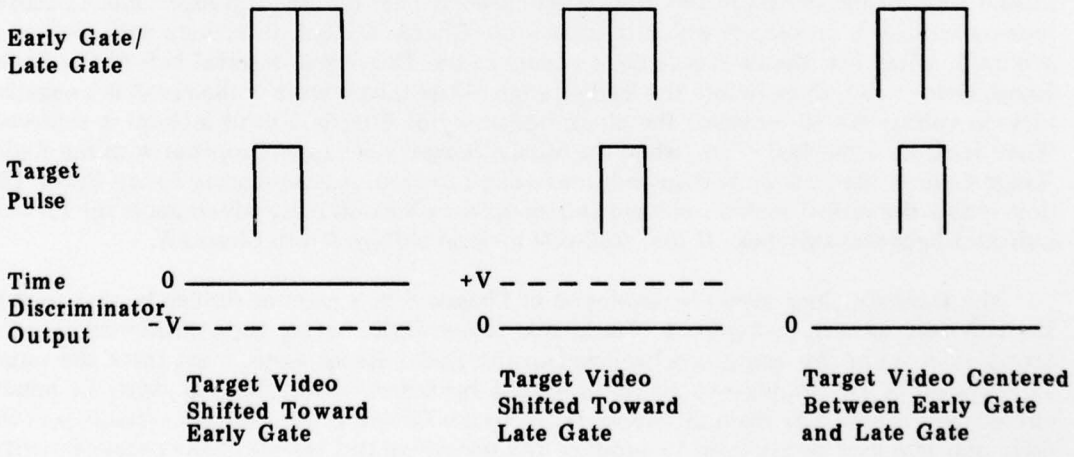


Figure 3. **TIME DISCRIMINATOR WAVEFORMS DURING INTERNAL TRACKING**

relocking on a target no matter how much phase shift has developed due to loss of video; however, this advantage is not achievable because the missile does not have the proper target-discrimination provisions to prevent locking on some extraneous radar reflection.

3.4 DETAILED CIRCUIT DESCRIPTIONS

Sections 3.4.1 through 3.4.7 provide detailed descriptions of the replacement-module circuits. For a complete schematic diagram, the reader is referred to ARINC Research Drawing No. D000376.

3.4.1 Voltage-Controlled Oscillator

The active elements for the Voltage-Controlled Oscillator are two inverter circuits contained in a type SN5404J hex inverter (six inverters in one package). The output of the oscillator is a 4-volt (nominal) square wave with a period controlled by a crystal (Y1) operating in its series resonant mode. Control of the frequency is achieved by the use of a voltage variable capacitance diode (VVC or varactor) connected in series with the crystal. Changes in the capacity of the VVC produce changes in the series resonant frequency of the crystal, thereby changing the output frequency of the oscillator.

Component values for the oscillator circuit (depicted in Figure 4) were chosen as follows:

(1) R_1 and R_3 are selected to bias the inverter inputs to a voltage as close as possible to the input voltage level at which switching from one logic level to the other takes place. This feature places the inverters in an unstable condition, ensuring reliable starting and a symmetrical waveform. (The symmetrical waveformis not important for this application, but symmetry is an indicator of optimum oscillator circuit performance.)

(2) C_1 is a coupling capacitor chosen for low reactance compared to amplifier input and output resistance.

(3) C_2 and C_3 are used to block the VVC control voltage to keep it from affecting the inverter bias voltages. Their capacitance values are at least 10 times the capacitance of the VVC.

(4) R_2 and R_4 provide (a) low resistance paths for the dc control voltage relative to the high back resistance of the VVC and (b) high resistance paths for the ac component relative to the low capacitive reactance of the VVC.

(5) Y_1 is the AT cut crystal which operates in its series resonant mode and stabilizes the frequency of the oscillator.

(6) CR1 is the Voltage Variable Capacitance diode (VVC) which exhibits a change in capacitance for a change in control voltage. Connected in series with the crystal, the VVC is used to deviate or pull the resonant frequency of the crystal, yielding a frequency-vs-voltage transfer function, as shown in Figure 5.

3.4.2 Frequency Dividers

The division from the high clock frequency to the radar pulse repetition frequency is accomplished in three integrated circuits, two being four-bit binary counters and one a decade counter. The type SN5493J binary counters provide a division by 16 (each) and the type SN5490J decade counter provides a division by 10. The total amount of frequency division is therefore $16 \times 16 \times 10$ or 2,560.

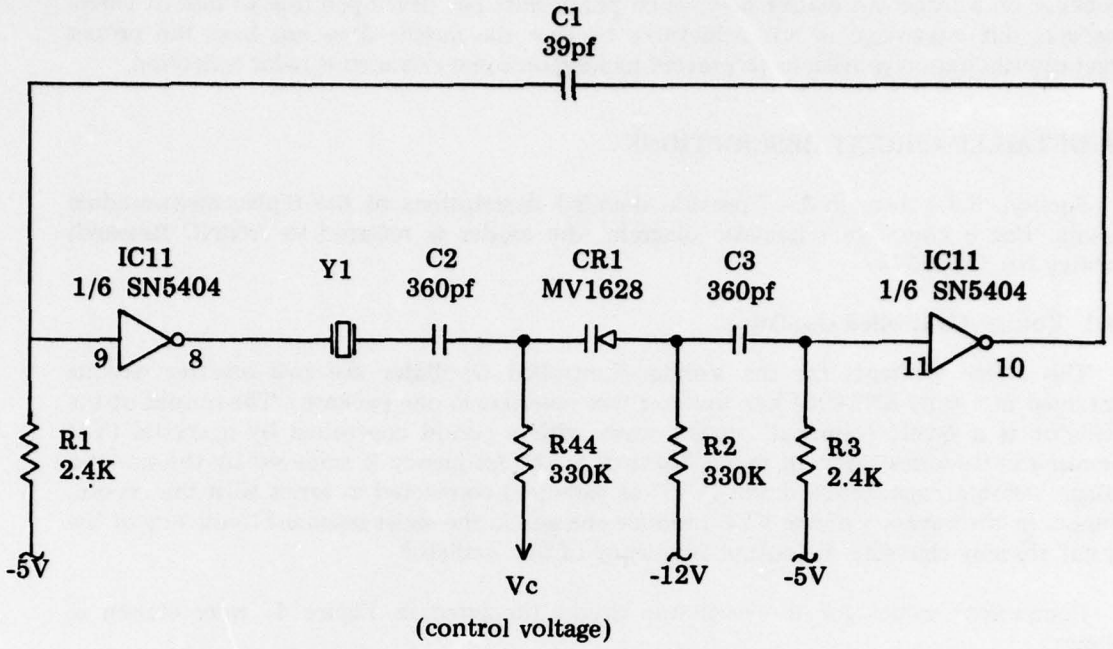


Figure 4. **VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT**

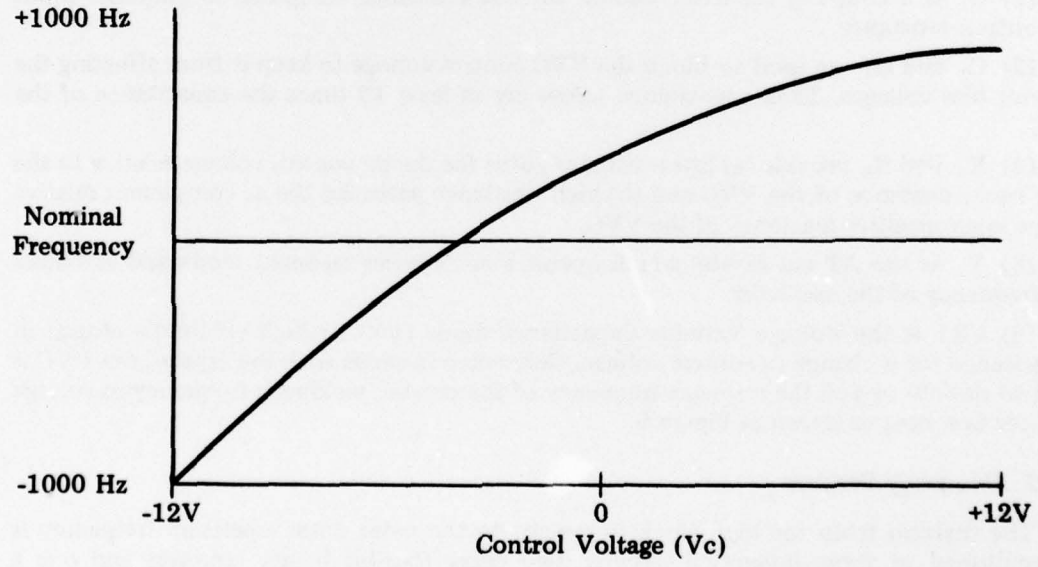


Figure 5. **VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT: FREQUENCY-VS-VOLTAGE TRANSFER FUNCTION**

The circuitry in each counter package consists of four transistor transistor logic (TTL) flip flops. TTL features high speed at the expense of higher current drain, as compared with DTL (diode transistor logic) and RTL (resistor transistor logic), the other popular logic types. Figure 6 is a schematic illustration of the counter circuits.

3.4.3 Range Gate Generators

The range gate pulses developed in Chassis 5 are used in two places: (1) the negative range gate enables the intermediate frequency (IF) amplifier chain in Chassis 6, and (2) the positive range gate triggers a "boxcar" error detector in Chassis 4. The positive and negative Range Gate Generators are shown schematically in Figure 7.

The IC5 one-shot diagrammed in Figure 7 produces a delay before starting the Range Gate Generators. This delay compensates for various system delays and allows the proper positioning of the early and late gates with respect to the range gates. IC6, another one-shot, produces the range gate pulse. The output of IC6 is approximately 4 volts in amplitude, and Q_2 and Q_3 are used to amplify the pulse to 40 volts for the positive range gate and 80 volts for the negative range gate. Q_1 and Q_2 are configured in active amplifier stages instead of switches to maximize switching speed by avoiding saturation and the consequent hole storage time.

Monostable Multivibrators

The type SN54121J Monostable Multivibrator used to perform various delay and pulse-forming functions in the solid-state Chassis 5 generates both a positive (Q output) and negative ($\overline{Q}$ output) pulse when triggered by the negative slope of an input waveform. The pulse duration (T) is controlled strictly by the external resistor (R) and capacitor (C) network connected between pins 10 and 11. The formula for pulse duration is $T = 0.694$ RC.

The SN54121J utilizes a combination of TTL (transistor transistor logic) circuits and thus can be directly coupled to other TTL circuits. The output peak-to-peak pulse level is approximately 4 volts.

3.4.4 Early and Late Gate Generators

The early and late gates which bracket the target video pulse during tracking are positioned by the delays produced by integrated circuits IC7 and IC8, and the actual gates are produced by IC9 and IC10, as illustrated in Figure 8. All four integrated circuits are type SN54121J one-shot circuits.

3.4.5 Time Discriminator Circuit

The Time Discriminator Circuit, illustrated in Figure 9, generates the analog error voltage that is proportional to the position in time of the target video pulse relative to the early and late gates. The early and late gate pulses are applied to Q_4 and Q_7, respectively, which serve as pulse amplifiers. Transformers T_3 and T_2 couple the pulses into the gate circuit of Q_5 and Q_6, the junction field-effect transistors which perform a coincidence function by allowing current to flow only when pulses are present at both the gate and drain terminals. Transformer T_1 receives the target video pulse (superimposed on the Missile Range Gate pedestal) and applies it to the drains of Q_5 and Q_6 via two separate secondary windings. Polarities of the floating Q_5 and Q_6 switches are so connected that early gate coincidence signals produce a negative output voltage and late gate coincidence signals produce a positive output (as measured across C28).

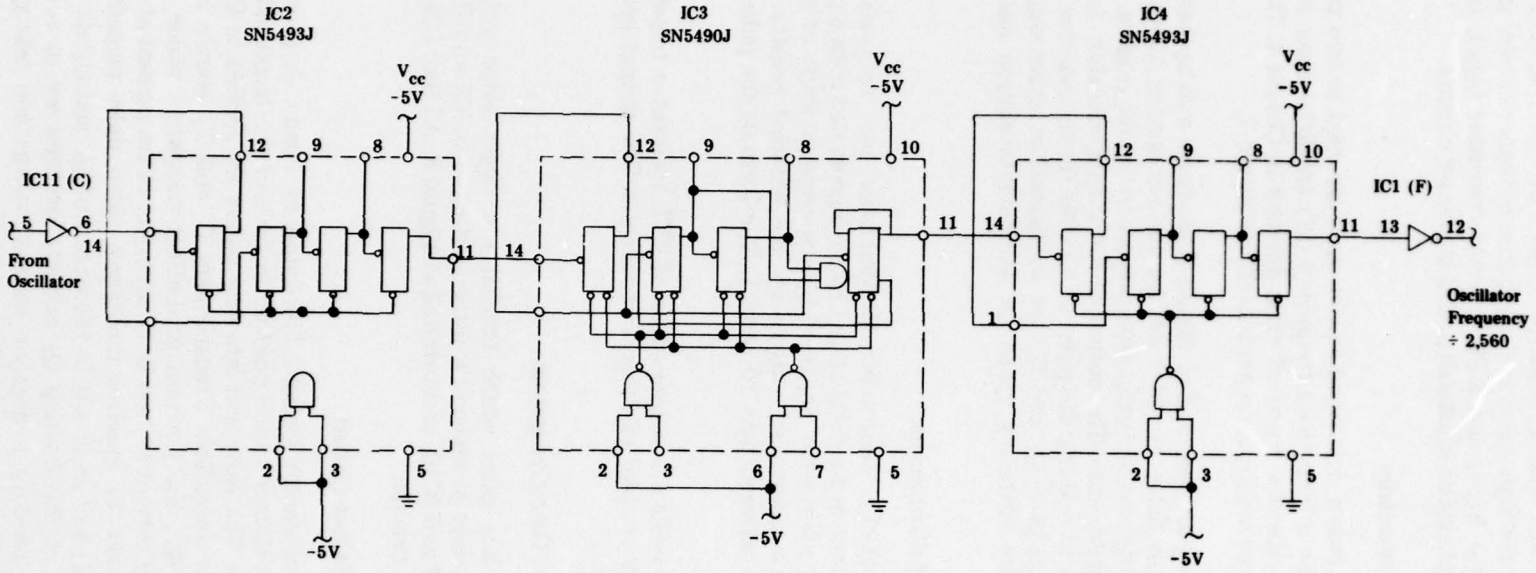


Figure 6. **COUNTER CIRCUIT**

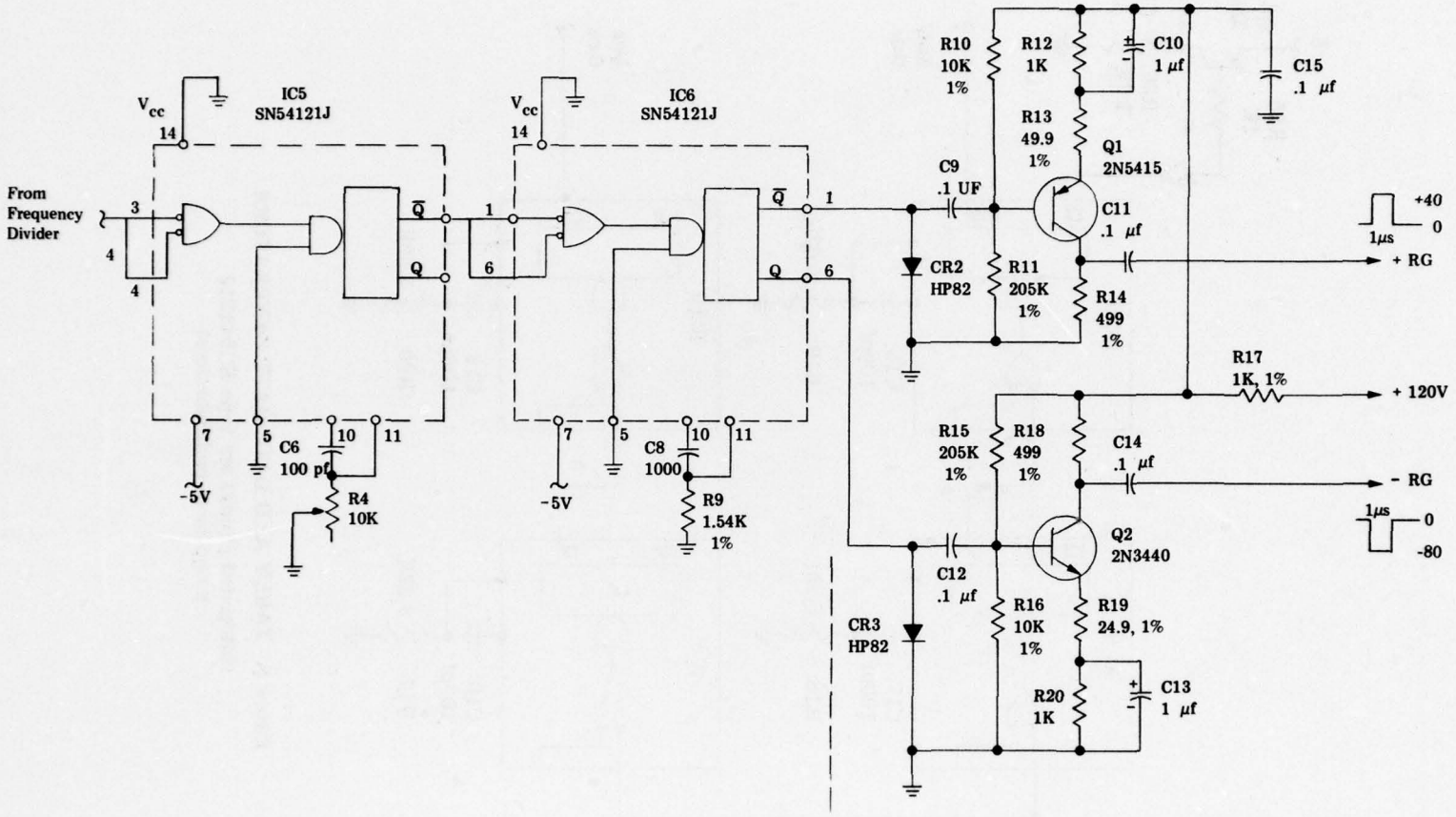


Figure 7. **POSITIVE AND NEGATIVE RANGE GATE GENERATORS**

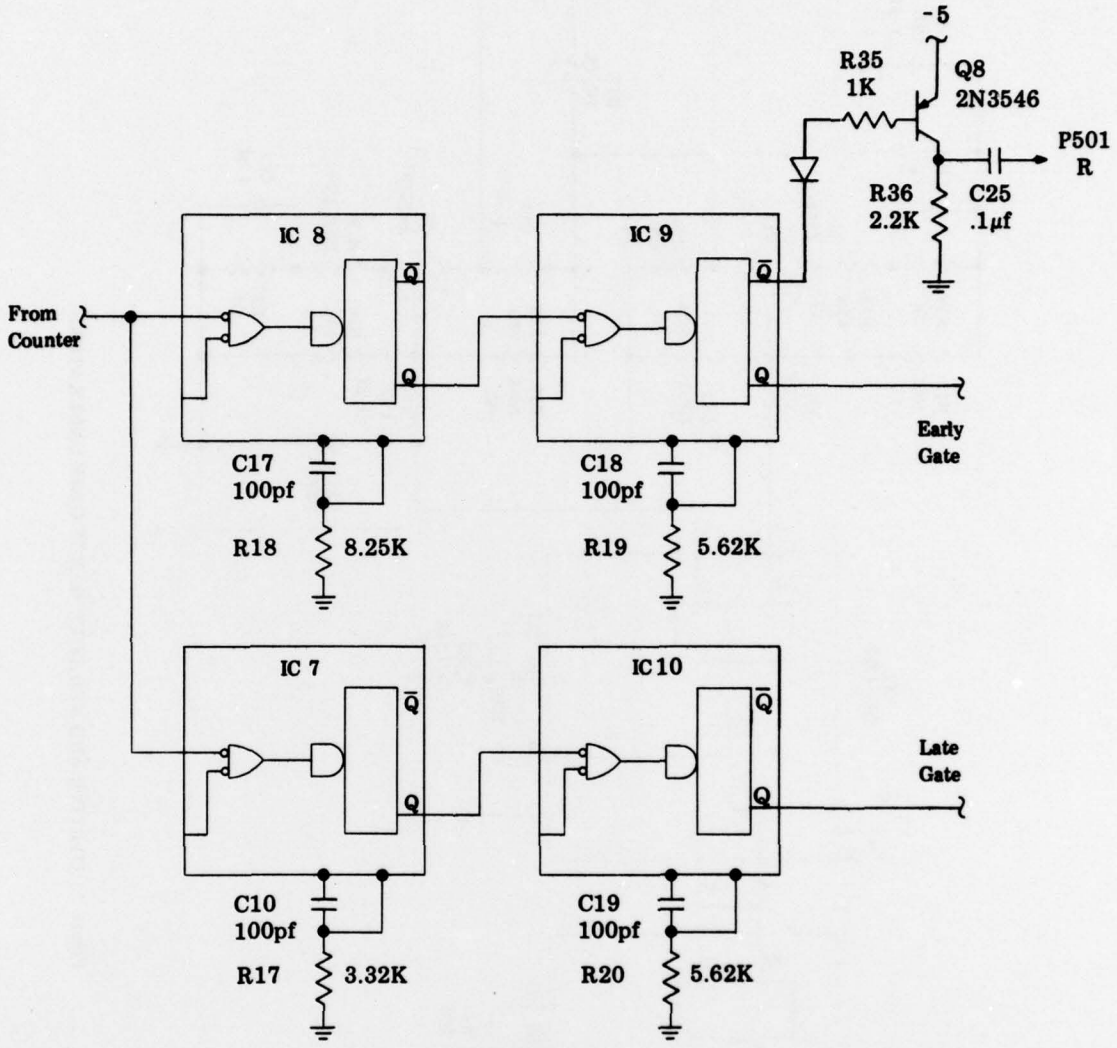


Figure 8. **EARLY AND LATE GATE GENERATORS**

(Integrated circuits are type SN54121J monostable multivibrators)

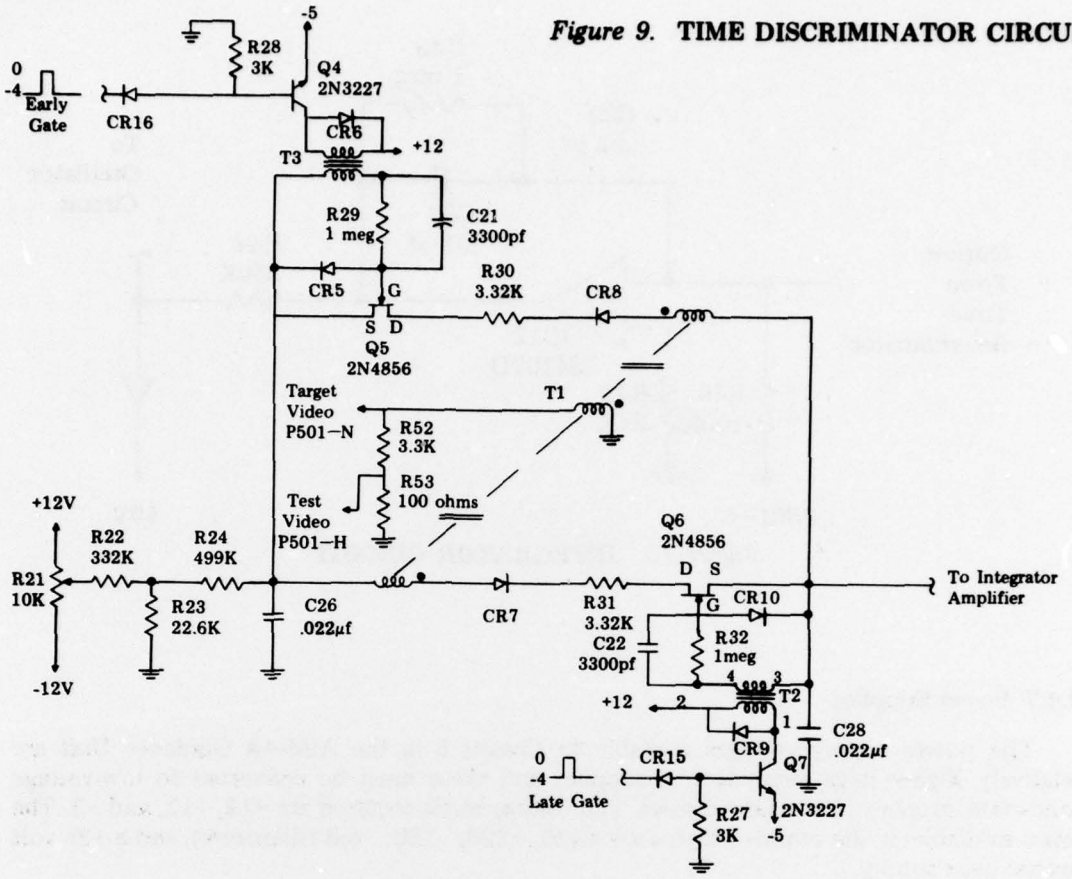


Figure 9. **TIME DISCRIMINATOR CIRCUIT**

In its analog aspect, the Time Discriminator Circuit provides an output voltage proportional to relative time coincidence of the video pulse with the early and late gates; however, the amplitude of this output is also affected by the amplitude of the video pulse. Thus the time discriminator exhibits a higher gain for larger target video pulses.

3.4.6 Integrator Amplifier

The Integrator Amplifier, diagrammed in Figure 10, produces an output voltage that is the integral of the input voltage as a function of time. This circuit filters the output of the time discriminator, provides the proper gain and phase lag to achieve the desired servo loop response, and enables the system to exhibit velocity memory.

The term "velocity memory" describes the characteristic of the system by which the Voltage-Controlled Oscillator maintains the frequency at which lock-on to the target was achieved even when the target pulse momentarily disappears. When the target reappears within the acceptance angle defined by the early and late gates, re-lock will be accomplished. Reacquiring a temporarily interrupted target pulse depends on (1) the target's maintaining a constant velocity relative to the missile and (2) the stability of Chassis 5 circuitry during the period when the target pulse is gone.

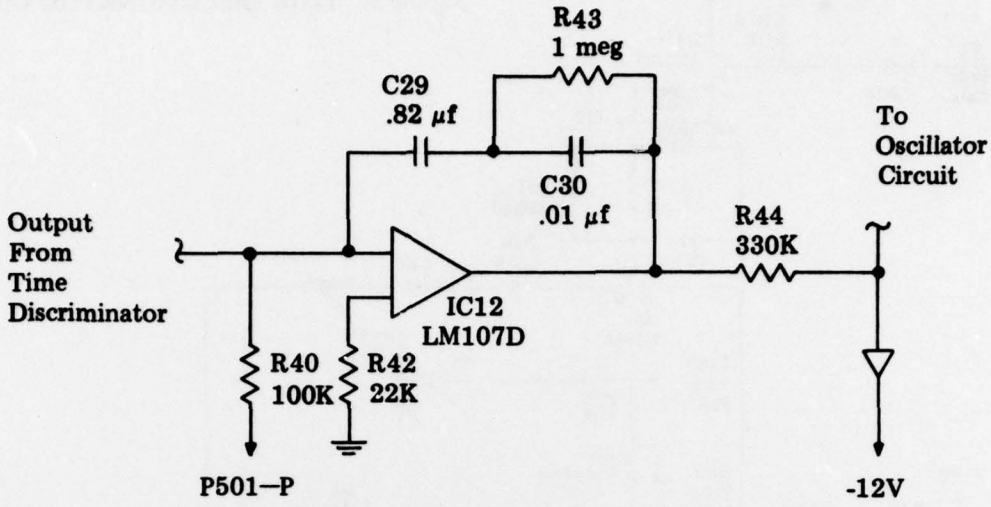


Figure 10. **INTEGRATOR CIRCUIT**

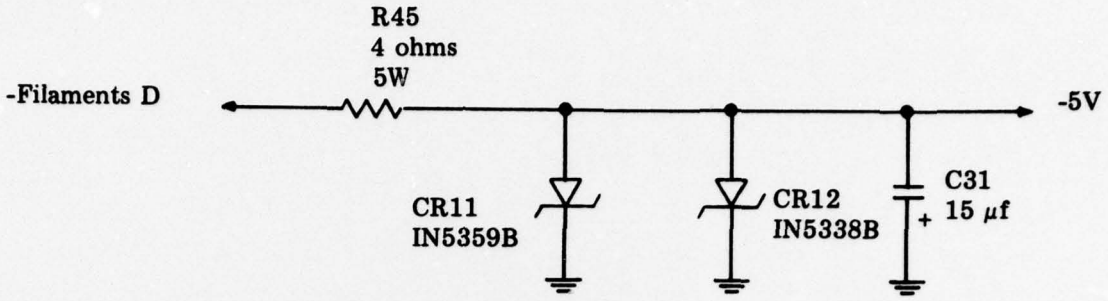
3.4.7 Power Supplies

The power supply voltages available to Chassis 5 in the AIM-4A Guidance Unit are relatively high-voltage vacuum-tube supplies and these must be converted to low-voltage solid-state supplies in the new chassis. The voltage levels required are +12, -12, and -5. The levels available at the connector pins are +120, +220, -150, -6.8 (filaments), and a +25 volt crystal oven supply.

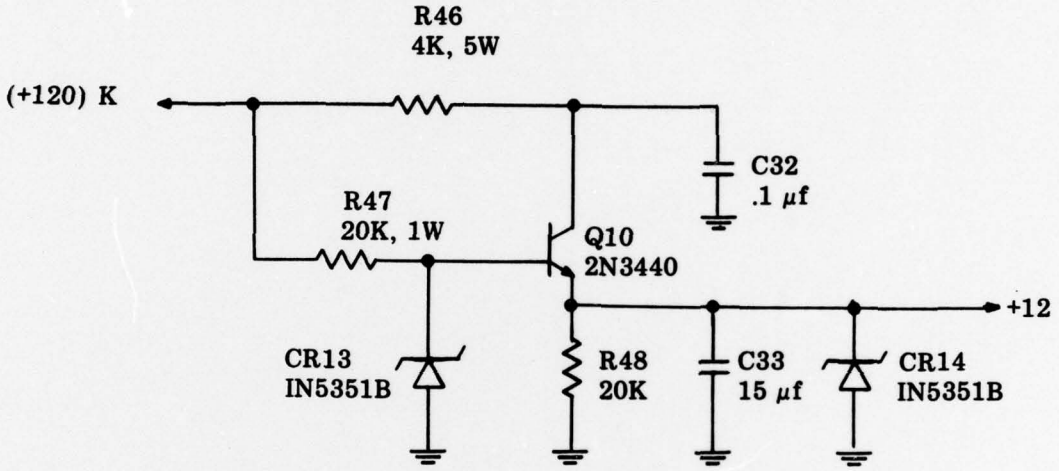
The +12 volt and -12 volt levels were developed by use of the emitter follower circuits shown in Figure 11. Zener diodes CR13 and CR17 provide voltage regulation and the emitter follower configuration limits the current variation in the zener diodes. Resistors R47 and R50 bias the zener diodes; R46 and R49 limit the power dissipation required of the transistors. Filtering is provided by capacitors C32, C33, C34, and C35, and zener diodes CR14 and CR18 are for protection of transistors and integrated circuits in the event of failure of CR13 and CR14.

The -5 volt supply is a simple zener diode regulator. The -6.7 volt filament level is dropped to -5 volts across resistor R45. Capacitor C31 provides filtering. Two zener diodes, CR 11 and CR 12, are used to enable the -5 volt supply to withstand "filament boost" — a condition that occurs when -10.8 volts is applied to the filament line for 10 seconds.

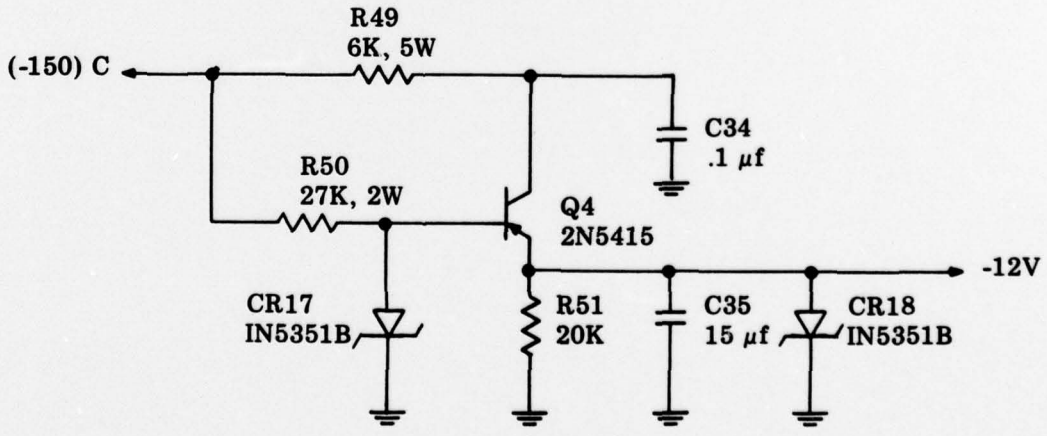
Capacitors C4, C5, C7, C27, C36, and C37 — shown on the Schematic Diagram, Drawing No. D000376 — are 0.01 μf capacitors electrically connected across power supply terminals and physically distributed throughout the chassis to locally suppress noise and unwanted transients.



-5 Volt Power Supply



+12 Volt Power Supply



-12 Volt Power Supply

Figure 11. **POWER SUPPLY CIRCUITS**

CHAPTER FOUR

TEST RESULTS

4.1 SYSTEM MOCK-UP

The mock-up used for Chassis 5 testing is described in block diagram form in Figure 12. Switch S1 simulates the breaking of the umbilical connection from the aircraft; it is closed for external slewing and opened for self-tracking. For the memory test, the negative pulse from the pulse generator to Chassis 6 is interrupted by a switch in the pulse generator.

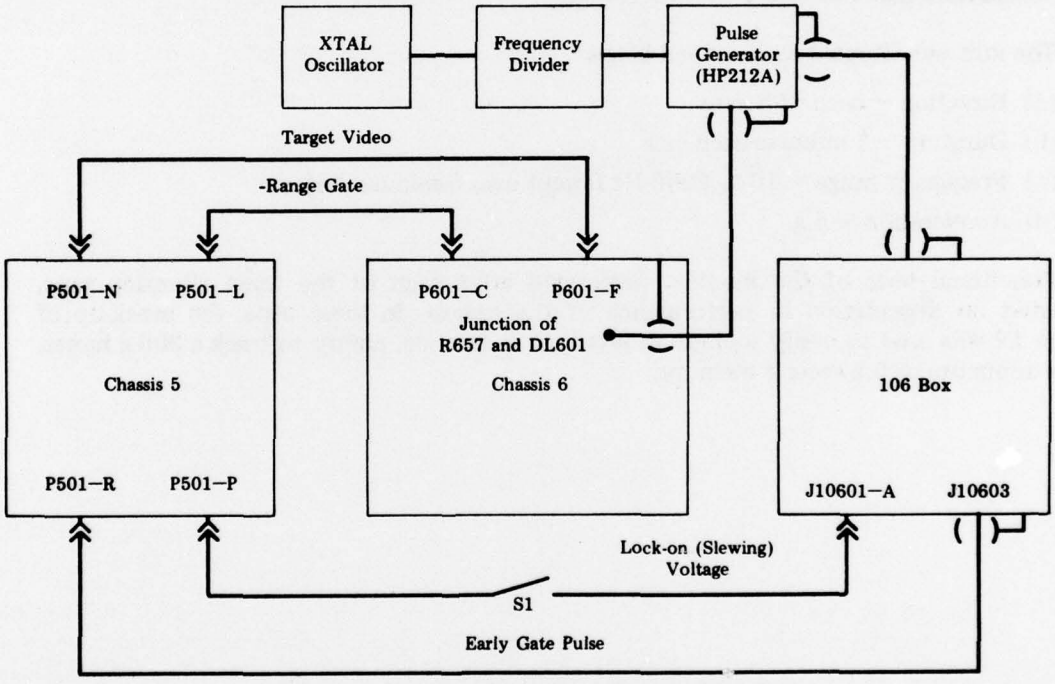


Figure 12. CHASSIS 5 TEST MOCK-UP

4.2 RESULTS OF TEMPERATURE TESTS

Prototype No. 1 was tested in a temperature chamber in the mock-up configuration illustrated in Figure 12.

The chassis locked on in less than 3 seconds and tracked a 300 g target over the temperature range of -20°F to +200°F. Performance was checked at 20°F intervals. A

rough estimate of memory capability was made over this temperature range and the following conclusions were drawn:

(1) If the drift potentiometer (R21) is adjusted at 90°F (midway between the temperature extremes), the 0.5-second requirement can be met over a ± 55°F range. At the temperature extremes, memory decreases to approximately 0.25 second.

(2) The dc contributors to memory loss, such as power supply drift and integrator amplifier offset drift with temperature, are not the primary causes of drift with temperature. The primary cause was found to be imbalances in the time discriminator.

(3) A vacuum-tube Chassis 5 tested under identical conditions demonstrated behavior similar to that of the solid-state chassis, as described in paragraph (1), above.

4.3 RESULTS OF VIBRATION TESTS

A nonoperating vibration test of the second and final prototype was performed in the ARINC Research Laboratory. The test was performed on the final unit — rather than the first unit, as originally planned — because the many modifications incorporated into the first unit would have made the test results unrealistic.

The unit was vibrated as described below:

(a) Direction — each of 3 axes

(b) Duration — 5 minutes each axis

(c) Frequency range — 10 to 2000 Hz (swept over 5-minute period)

(d) Acceleration — 5 g

Functional tests of the module, performed after each of the three vibration runs, indicated no degradation in performance of the chassis. In these tests, the mock-up of Figure 12 was used to verify lock-on in less than 3 seconds, ability to track a 300 g target, and a minimum of 0.5 second memory.

CHAPTER FIVE

CONCLUSIONS AND RECOMMENDATIONS

On the basis of the work described in this report, ARINC Research Corporation submits the following conclusions and recommendations:

(1) Laboratory tests have indicated that the solid-state Chassis 5 is a direct replacement for the vacuum-tube chassis.

(2) Further tests, including flight tests, should be performed to further verify the adequacy of the design.

(3) A sample of approximately 10 units should be built for the purposes of:

   (a) developing production and acceptance-test techniques

   (b) testing the reliability of the module by accumulating flight-test time.

APPENDIX A

NOMINAL INTERNAL WAVEFORMS

(This appendix contains information classified CONFIDENTIAL; it is being submitted to Warner Robins Air Materiel Area by separate transmittal letter.)

APPENDIX B

CHASSIS 5 INTERFACE CHARACTERISTICS

1. Negative Range Gate

Pin	501-L
Amplitude	-80 ± 4 volts
Duration	1 ± 0.2 μs (measured at 50% amplitude points)
Source resistance	500 ohms
Coupling	0.1 μf capacitor

2. Positive Range Gate

Pin	501-B
Amplitude	40 ± 2 volts
Duration	1 ± 0.2 μs (measured at 50% amplitude points)
Source resistance	500 ohms
Coupling	0.1 μf capacitor

3. Early Gate

Pin	501-R
Amplitude	3 ± 0.5 volts
Duration	0.4 ± 0.1 μs
Source resistance	less than 100 ohms
Coupling	0.1 μf capacitor

4. Current Drain (Nominal)

-6.8 volts (filaments)	420 milliamperes
+120 volts	23 milliamperes
-150 volts	14 milliamperes

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Under Contract F09603-71-A-3749-0004, ARINC Research Corporation has designed and tested a replacement module for Chassis 5 in the AIM-4A guidance unit. The replacement incorporates both integrated circuits and transistors, and was designed to be directly interchangeable with the vacuum tube chassis without the necessity of other system modifications.

Two prototype models of the redesigned chassis were fabricated. Testing included functional and environmental tests. Captive flight tests of the prototype are planned for a later time. The functional and environmental tests have in-

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dicated that the solid-state module is a direct replacement for the vacuum-tube model.